on-chip inductor 10

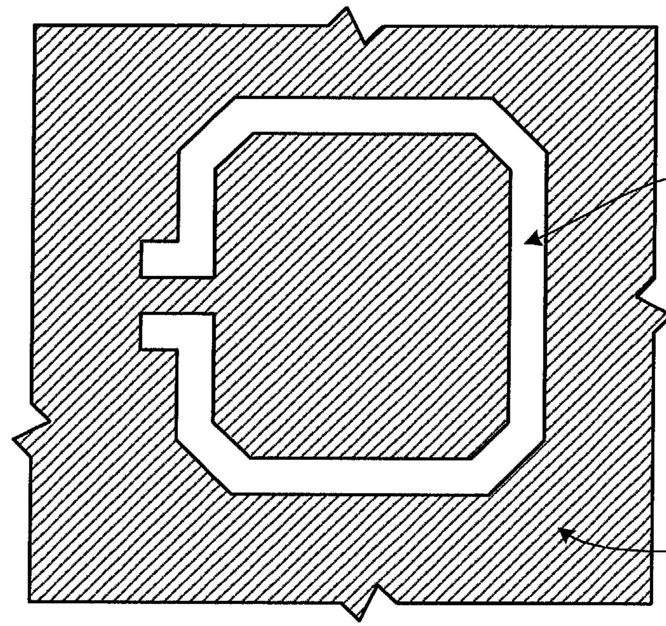

FIG. 1A
top view

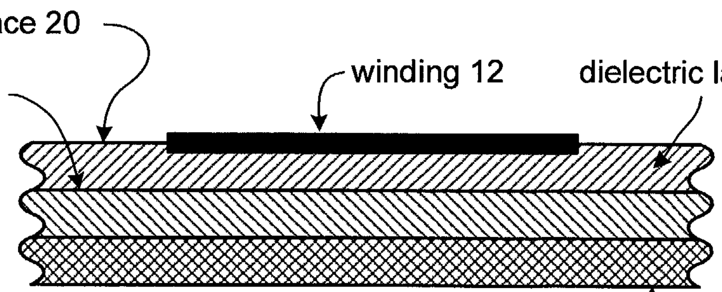

FIG. 1B
side view

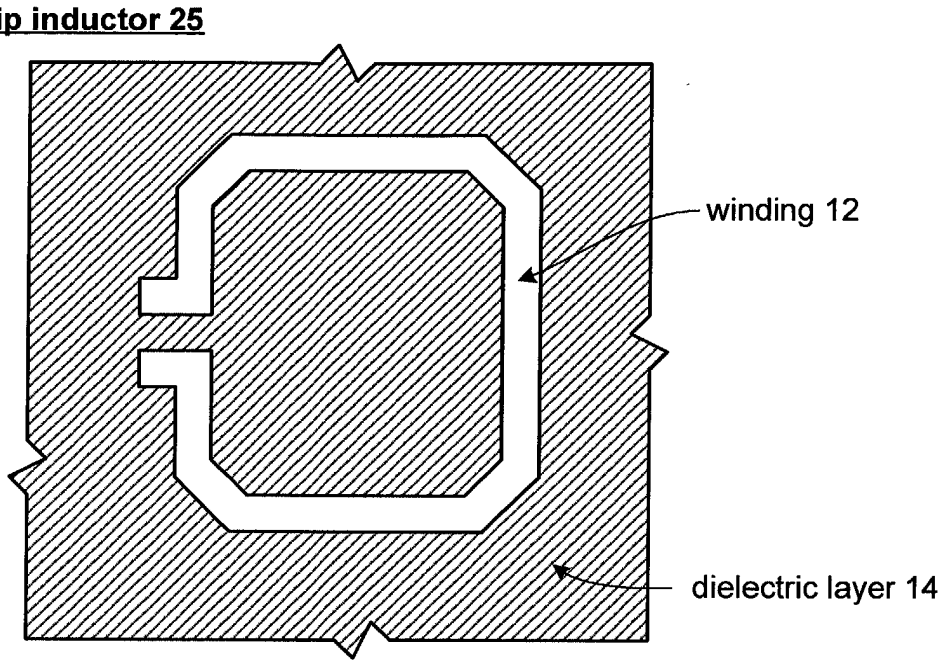

FIG. 2A
top view

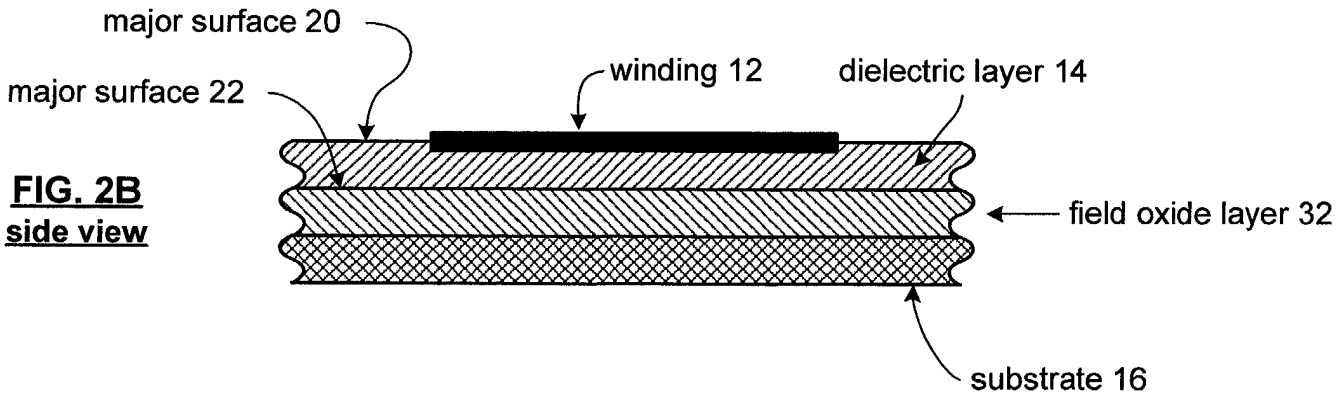

FIG. 2B
side view

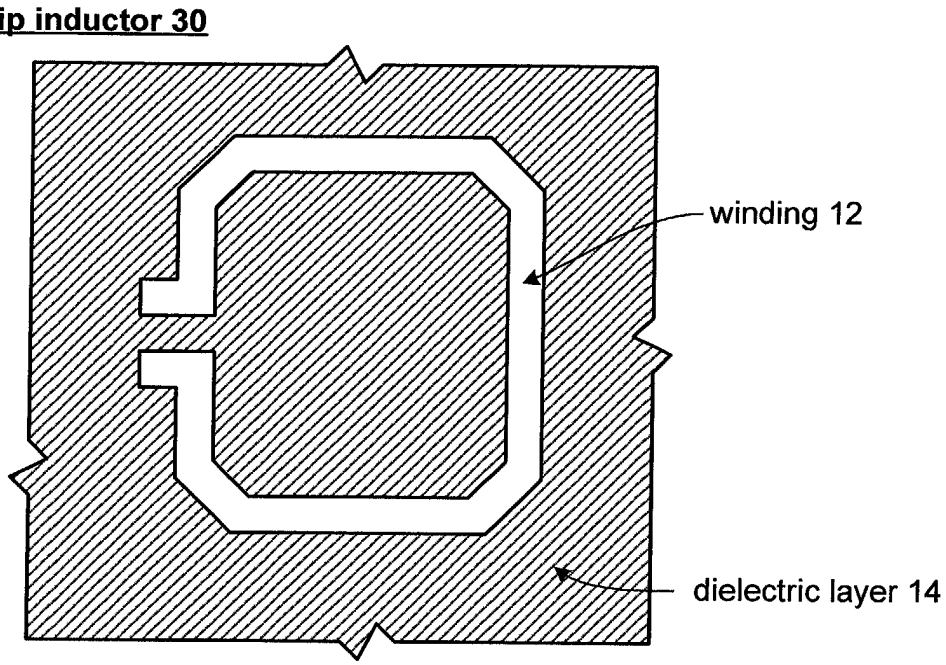

FIG. 3A
top view

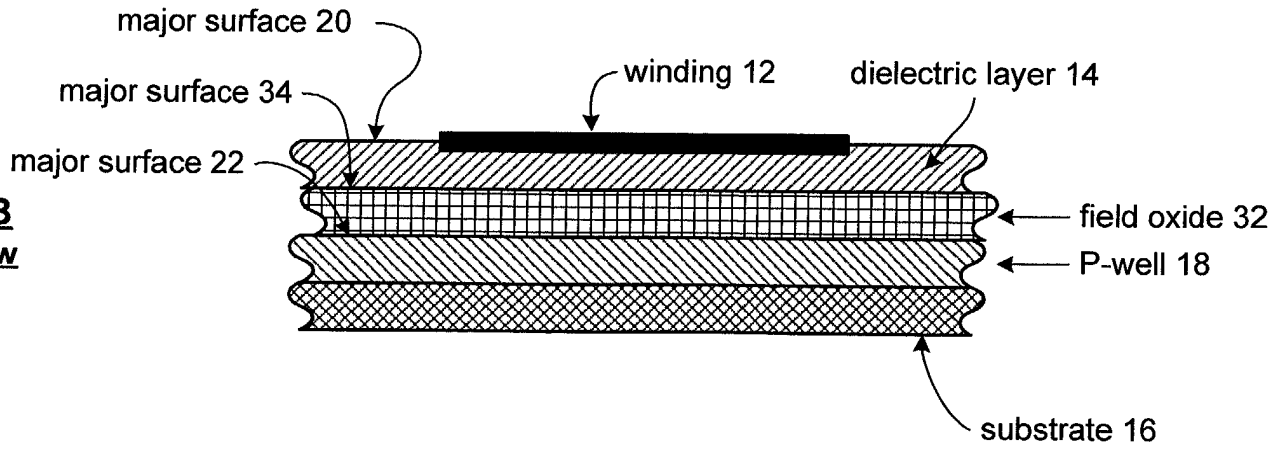

FIG. 3B
side view

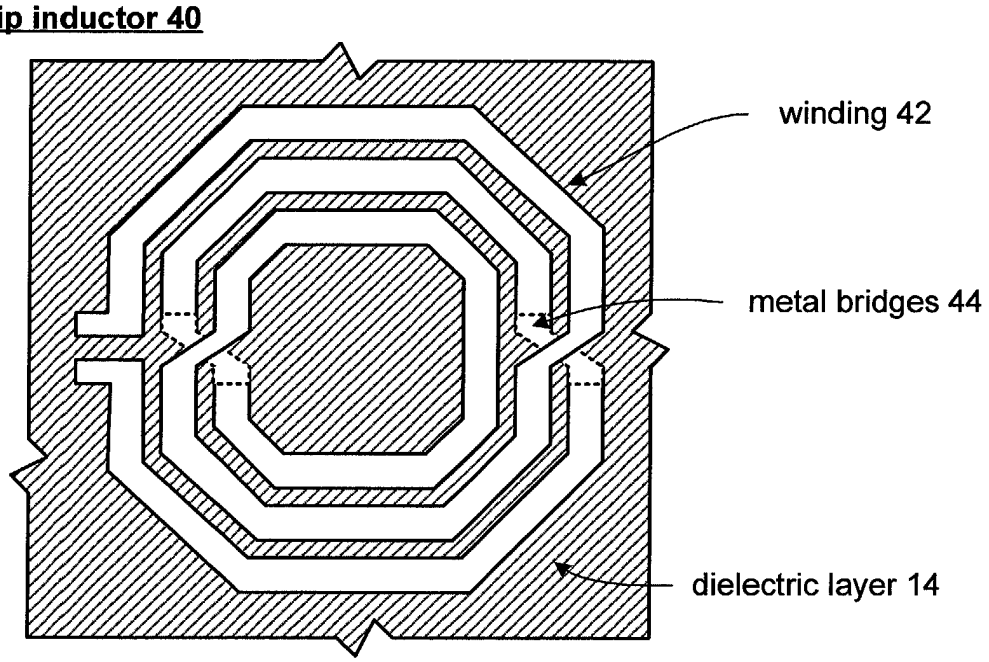

FIG. 4A
top view

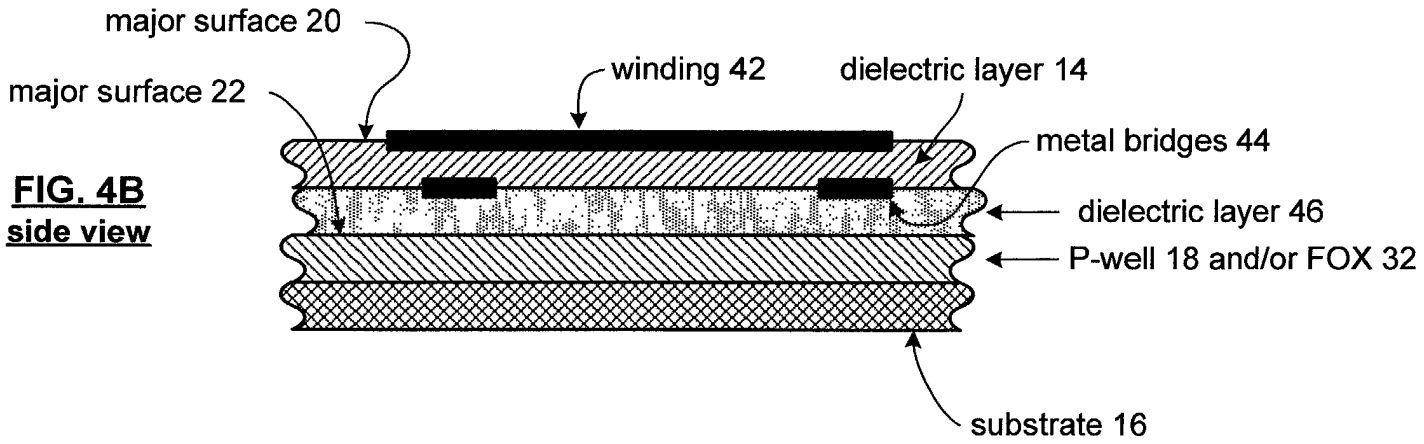

FIG. 4B
side view

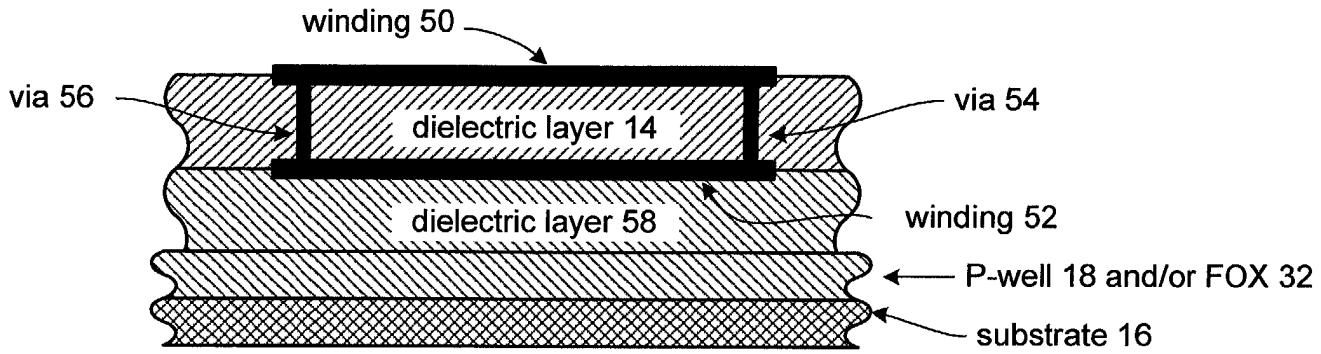

FIG. 5

differential inductor 60

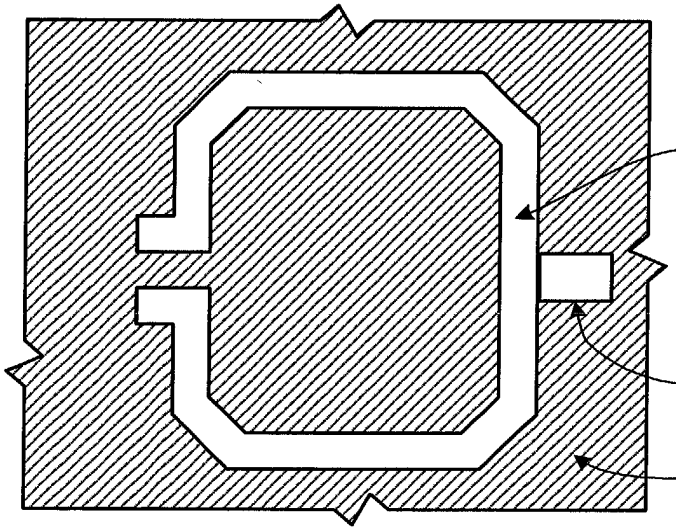

FIG. 6A
top view

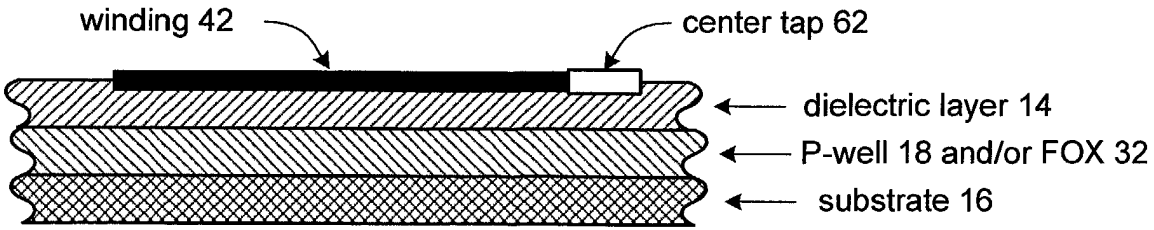

FIG. 6B
side view

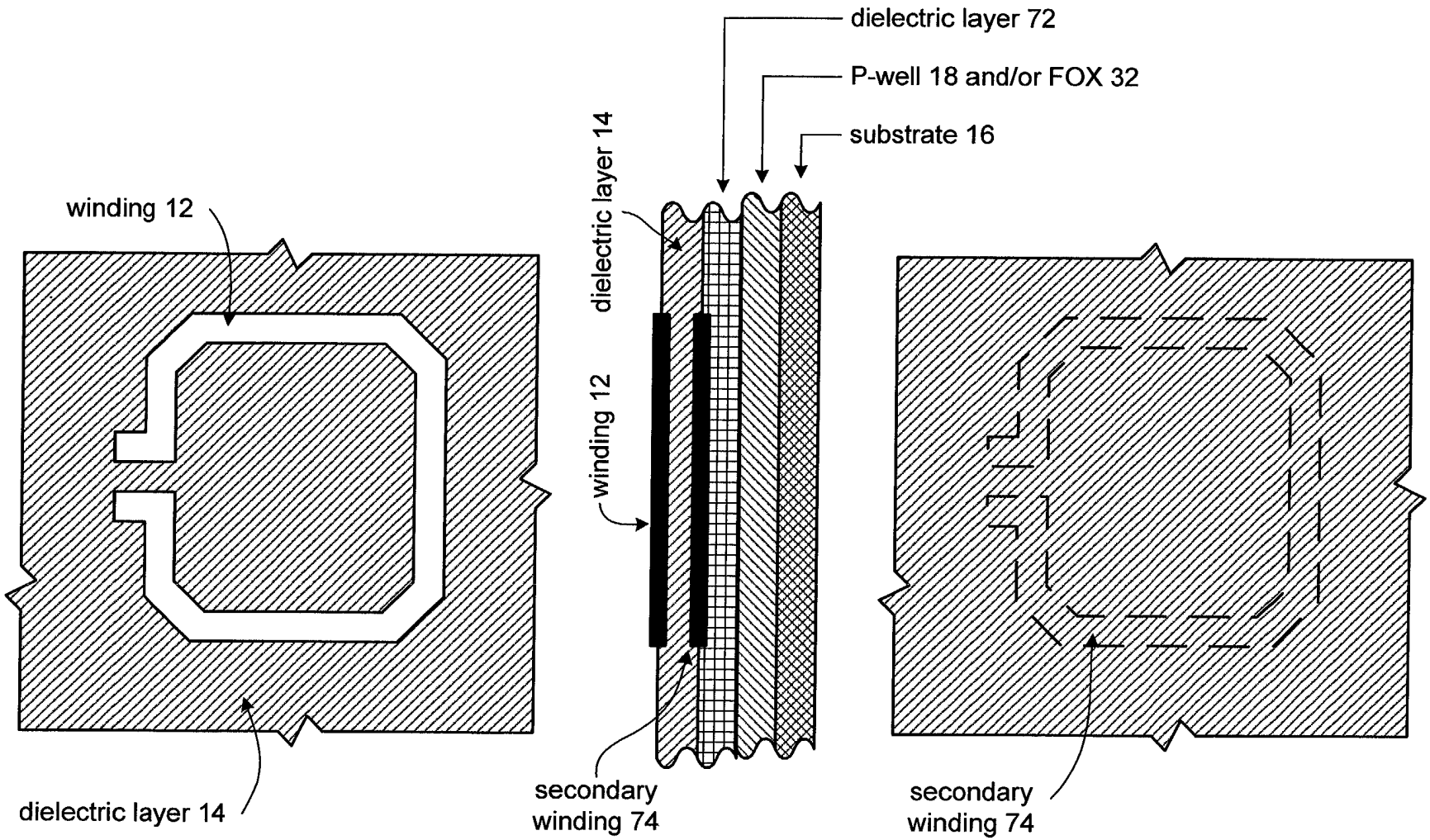

FIG. 7A
top view

FIG. 7B
side view

FIG. 7C
bottom view

on-chip transformer 70

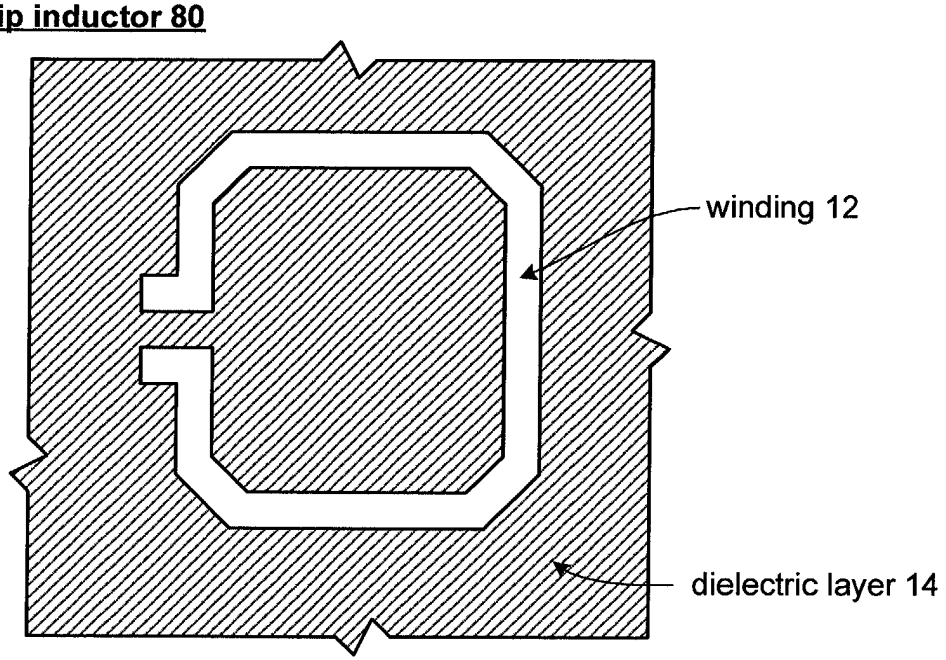

FIG. 8A
top view

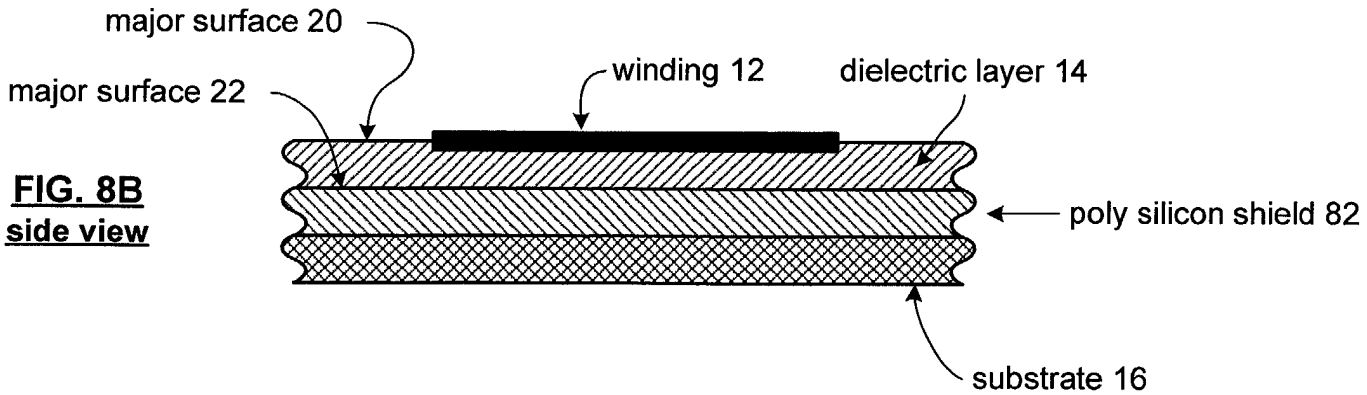

FIG. 8B
side view

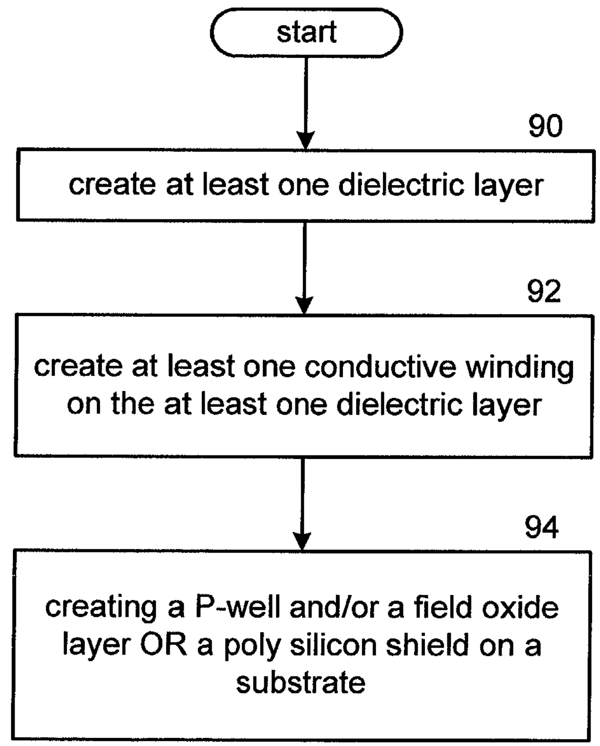
start
90
create at least one dielectric layer
92
create at least one conductive winding on the at least one dielectric layer
94
creating a P-well and/or a field oxide layer OR a poly silicon shield on a substrate

FIG. 9